

## REMARKS

In an Office Action mailed on January 24, 2006, claims 41-51, 53-60, 62-65 and 67 were rejected under 35 U.S.C. § 112, first paragraph; claims 54-60 were rejected under 35 U.S.C. § 112, second paragraph; objections were made to claims 41 and 62; and claims 41, 42, 45, 48, 49, 51, 53-55, 58-60, 62-65 and 67 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Arai and Yoshizawa. Independent claims 41 and 62 have been amended to overcome the corresponding claim objections. Claim 54 has also been amended to overcome the corresponding § 112, second paragraph rejection. The §§ 103 and 112 rejections are addressed below.

### § 112, First Paragraph Rejections:

Independent claims 41, 54 and 62 stand rejected under the first paragraph of § 112 because the specification allegedly fails to comply with the enablement requirement. However, Applicant directs the Examiner's attention to the language on page 5 of the application. In this regard, on page 5, the specification discusses the memory configuration routine 112 as determining a total memory capacity for the system. The specification states that this function may either be performed by BOS routines or alternatively, may be readily available on a non-volatile storage device such as the device 114. On page 5, the specification also discusses that if the system memory 110 includes RAMBUS® devices, there is a limit of 32 devices per memory channel. Additionally, on page 5, the specification describes that an additional limitation is that a RAMBUS® memory controller may only support three module sockets. Once again, this information may be stored in the non-volatile memory.

Thus, the specification clearly enables one skilled in the art to determine a maximum number of memory devices that can be supported per memory bus channel of a computer system. In the specific embodiments described in the specification, one such technique may be, for example, the prior knowledge that there is a limit of 32 devices per memory channel, and this information may be stored in a non-volatile storage device. Additionally, regarding independent claim 54, the specification clearly describes at least one embodiment to determine a memory capacity including a determining a maximum number of device sockets that can be supported by a memory controller. Therefore, Applicant requests reconsideration of the § 112, first paragraph

rejections due to the alleged non-enablement, as the specification clearly describes at least one way to determine the maximum number of memory devices that can be supported per memory bus channel, i.e., reading this information from a non-volatile memory or using a BIOS routine.

Regarding the § 112, first paragraph rejections due to the alleged lack of written description, Applicant refers the Examiner to page 5 of the specification and the language cited above. In the regard, it is clear that Applicant had possession of the invention at the time the application was filed, as the specification outlines at least one embodiment to determine a memory capacity by determining a maximum number of memory devices that may be supported per memory bus channel and determining a memory capacity by determining a maximum number of device sockets that may be supported by a memory controller. Therefore, for similar reasons, Applicant supports that independent claims 41, 54 and 62 comply with the written description requirement.

For at least the reasons that are set forth above, Applicant requests withdrawal of the § 112, first rejections of claims 41-51, 53-60, 62-65 and 67.

#### § 103 Rejections:

The Examiner has failed to establish a *prima facie* case of obviousness for any of the § 103 rejections for at least the reason that the hypothetical combination of Arai and Yoshizawa fails to teach or suggest the missing claim limitations.

More specifically, the Examiner relies on the RAMBUS data sheet and more particularly refers the Applicant to page 40. On page 40, the RAMBUS data sheet describes configuration options of the RAMBUS device that may be read from memory. However, even assuming, for purposes of argument, that the configuration of options disclosed in the RAMBUS data sheet are inherent in Arai, page 40 of the RAMBUS data sheet fails to disclose any configuration information regarding the maximum number of devices per memory bus channel, as this knowledge was supposedly known by the designer of Arai's computer system. Thus, there is no reason why Arai's system would need to know this information. Therefore, even assuming that the limitations that are presented in the RAMBUS data sheet are inherent in Arai, there is still no teaching or suggestion for executing a software routine to determine a maximum number of

memory devices that can be supported per memory bus channel and automatically determine memory upgrade options based on the determined memory capacity.

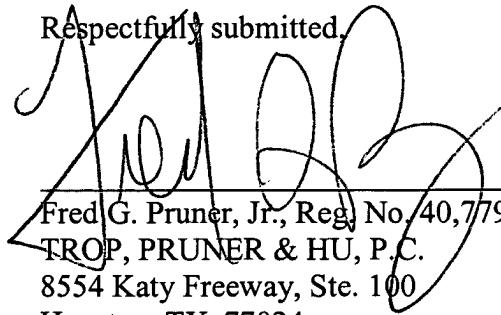
Regarding independent claim 54, page 40 of the RAMBUS data sheet, likewise fails to teach or suggest any configuration that indicates the maximum number of device sockets that can be supported by a memory controller. Therefore, even assuming that the limitations of the RAMBUS data sheet are incorporated into Arai, there is no teaching or suggestion in Arai or Yoshizawa regarding determining memory upgrade options based on a memory capacity that is determined by executing instructions to determine a maximum number of device sockets that can be supported by a memory controller. Without this showing, a *prima facie* case of obviousness has not been established for independent claim 54.

Therefore, for at least the reasons that are set forth above, Applicant requests withdrawal of the § 103 rejections of claims 41-51, 53-60, 62-65 and 67.

#### CONCLUSION

In view of the foregoing, withdrawal of the §§ 103 and 112 rejections and a favorable action in the form of a Notice of Allowance are requested. The Commissioner is authorized to charge any additional fees, or credit any overpayment to Deposit Account No. 20-1504 (MCT.0102US).

Respectfully submitted,



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